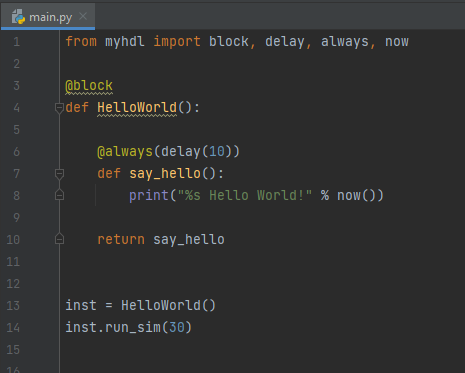
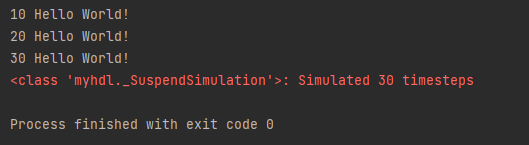
**Introduction to MyHDL**

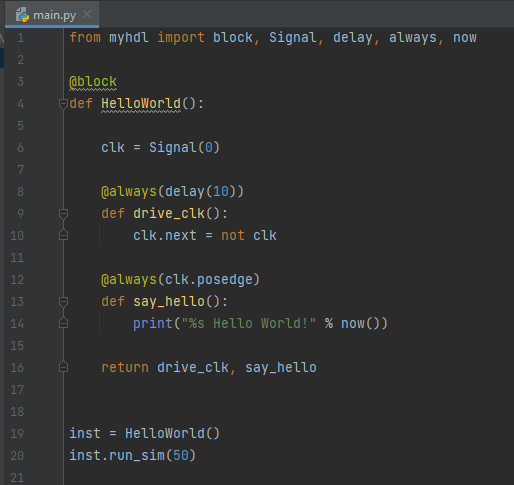
**A basic MyHDL simulation**



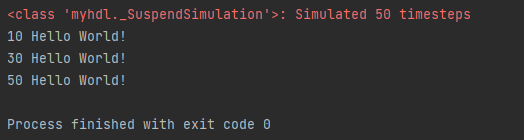
Po uruchomieniu symulacji otrzymano:



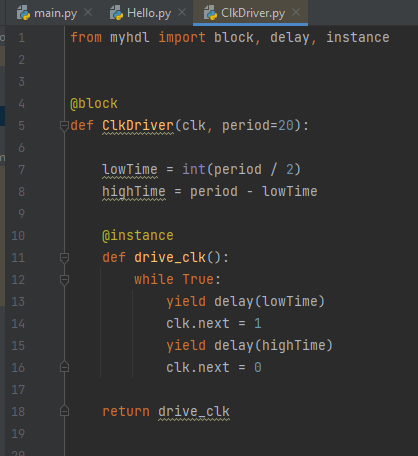
**Signals and concurrency**

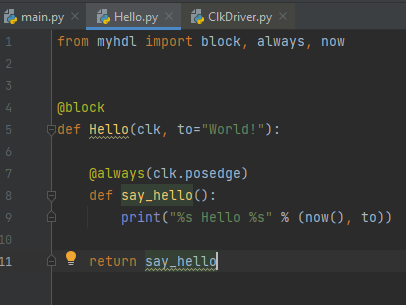


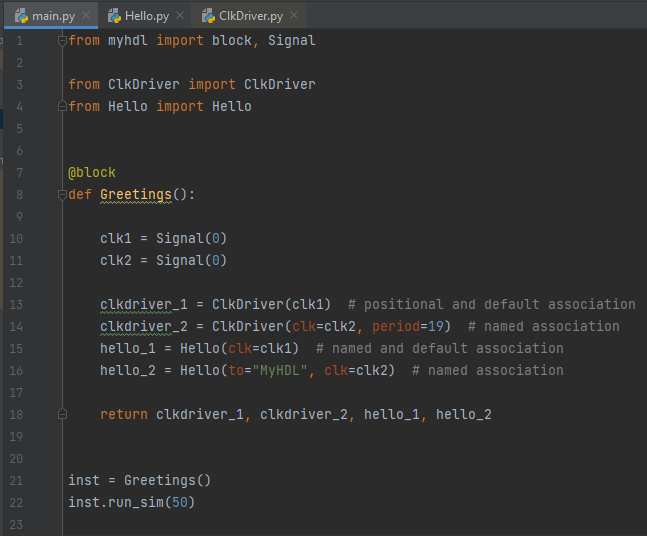
Po uruchomieniu symulacji otrzymano:



## Parameters, ports and hierarchy







Po uruchomieniu symulacji otrzymano:

